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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/736,934	12/16/2003	Hisashi Yamauchi	NEC 15.938A	5519

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EXAMINER	
LAMARRE, GUY J	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 10/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/736,934	YAMAUCHI	
	Examiner	Art Unit	
	Guy J. Lamarre, P.E.	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/265,346.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *16 Dec. 2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

0. Applicant's pre-amendment of 30 Dec. 2003 and IDS of 16 Dec. 2003 have been entered. The Examiner has considered the IDS.

0.1 Pursuant to 35 USC 131, **Claims 1-4** are presented for examination.

Reassignment Affecting Application Location

1. The Art Unit location of your application in the USPTO has changed. To aid in correlating any papers for this application, all further correspondence regarding this application should be directed to Art Unit 2133.

Claim Rejections - 35 USC ' 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.1 **Claims 1-4** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Applicants' Admitted prior art** (hereinafter **Admitted prior art**) in view of **Schilling et al.** (ELECTRONIC CIRCUITS: Discrete and Integrated, 1979; pages 560-615).

As per Claims 1-2, 4 Admitted prior art substantially discloses the procedure for the claimed method of generating test patterns, comprising (a) counting or identifying means (page 4 line 7); (b) checking noise value means (page 4 line 16); (c) selecting means to make process fall within allowable noise range (page 4 line 20); (d) changing input pattern based on step (c) (page 4 line 21). {See **Admitted prior art,** Fig.19, and page 1 line 8 – page 4 line 17, in passim, wherein apparatus and method are described.} **Not specifically described** in detail in **Admitted prior art** is the step whereby processing is performed based on circuit component noise margin and fan-out/fan-in requirement adjustments.

However such noise margin and fan-out design requirement approach is well known in electronics communications devices wherein such design requirements are taken into consideration so as to allow for or permit adequate component bias/operational voltage swings. For example, **Schilling et al.,** in an analogous art, discloses a synopsis on "Logic Gates" wherein such techniques are described. {See **Schilling et al.,** Id., Figs 12.1-3 and 4, pages 564-565.}

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the procedure of the **Admitted prior art** by including therein a noise margin and fan-out design method as taught by **Schilling et al.,** because such modification would provide the procedure disclosed in the **Admitted prior art** with a technique whereby "*the upper limit on the fan-out is determined by the tolerable values of voltages and currents,*" thus allowing the circuit designer to select electrical component parameters accordingly. {See **Schilling et al.,** page 565, penultimate para.}

As per Claim 3, Schilling et al. discloses the procedure for the claimed method of claim 1 further comprising repeated counting means. {See **Schilling et al.,** Figs. 12.1-3 and 4, wherein means is provided for selecting and counting.}

Drawings

3. The Drawings are objected to because Figure 19, referred to as conventional in the specification, has not been labeled as prior art. Appropriate correction is required.

Claim Rejections - 35 USC § 112 SECOND PARAGRAPH

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4.1 **As per Claim 1:** there is a lack of antecedent basis in last limitation for "the input pattern" for such had been previously defined.

4.2 **As per Claim 4**: the 1st process is missing, and thus there is a lack of antecedent basis for such in the rest of said claim.

Response to Arguments

5.0 Applicants' arguments concurrently filed have been fully considered, but they are not persuasive.

REMARKS

5.1 In response to **Claims 1-4,** Applicants, on page 5 para. 3, allege that "*the present invention relates to a method to generate the input pattern set in the scan cells as a test pattern for the internal circuit of the LSI, the test pattern preventing a noise problem.*"

Examiner disagrees as such recitation is not incorporated into the claim language. 'Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).'

Conclusion

5.2 The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

5.3 Any response to this action should be mailed to:

Commissioner of Patents and Trademarks, Washington, D.C. 20231

or faxed to: (703) 872-9306 for all formal communications.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Guy J. Lamarre, P.E., whose telephone number is (703) 305-0755. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert De Cady, can be reached at (703) 305-9595.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Information regarding the status of an application may also be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Guy J. Lamarre, P.E
Primary Examiner
10/13/04